UNITED STATES PATENT APPLICATION

FOR

CAPACITIVE ULTRASONIC TRANSDUCERS WITH ISOLATION POST

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BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to capacitive of micromachined ultrasonic transducers (cMUTs) and more particularly to a capacitive micromachined ultrasonic transducers having a patterned isolation layer which prevents shorting of the electrodes during operation and reduces the total number of trapped charges as compared to a non-patterned isolation layer.

BACKGROUND OF THE INVENTION

Ultrasonic transducers have been used in a number of sensing applications such as medical imaging non-destructive evaluation, gas metering and a number of ultrasound generating applications such medical therapy, industrial cleaning, etc. One class of such transducers is the electrostatic transducers. Electrostatic transducers have long been used for receiving and generating acoustic waves. Large area electrostatic transducer arrays have been used for acoustic imaging. The electrostatic transducers employ resilient membranes with very little inertia forming one electrode of the electrostatic transducers with the electrodes supported above a substrate which forms the second electrode. When distances between the electrodes are small the transducers can exert very large forces against a fluid in contact with the membrane. The momentum carried by approximately half a wavelength of air molecules in contact with the upper surface is able to set the membrane in motion and vice versa. Electrostatic actuation and detection enables the realization and control of such membranes.

Broad band microfabricated capacitive ultrasonic transducers (cMUTs) may include multiple elements each including membranes of identical or different sizes and shapes supported above a silicon substrate by walls of an insulating material which together with the membrane and substrate define cells. The walls are formed by micromachining a layer of insulation material such as silicon oxide, silicon nitride, etc. The substrate can be glass or other substrate material. The capacitive transducer is formed by a conductive layer on the membrane and conductive means such as a layer either applied to the substrate or the substrate having conductive regions. A single cell of a cMUT is illustrated in Figure 1. The cMUT includes a bottom electrode 11 and a top electrode or membrane 12 supported by insulating walls 13. When suitable AC and DC voltages are applied between the electrodes electrostatic forces cause the membrane to oscillate and generate acoustic waves. Alternately a DC voltage applied between the electrodes can be modulated by oscillation of the membrane resulting from sound waves stricking the membrane. The cMUT includes an isolation layer 14 such as an oxide layer

to prevent shorting between the electrodes if the membrane is deflected into contact the bottom wall of the cell 16.

The electric field between the electrodes can attract and trap charges 17 either on the surface of or in the insulating layer 14. The charges stay in the trapping cites for a long period because there is no DC path to discharge them. The accumulated charge shifts the DC voltage between the two electrodes away from the applied voltage by a random value. This dramatically degrades the reliability and repeatability of device performance.

OBJECTS AND SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide cMUTs in which trapped charges are minimized.

It is a further object of the present invention to provide cMUTs in which isolation is provided by spaced isolation areas or posts.

It is a further object of the present invention to provide isolation areas or posts at different locations and with different heights to allow the design and engineering of variation of the capacitance of the cMUT as a function of applied voltage.

There it is provided cMUTs which comprise a bottom electrode, a top membrane electrode, supported space from the bottom electrode by insulating walls and at least one isolation post or area disposed on the top or bottom electrode to limit the deflection of the top electrodes so that it does not contact the bottom electrode and to minimize the number of trapped charges.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more clearly understood from the following description when read in conjunction with the accompanying drawings of which:

Figure 1 is a sectional view of a single cell of a cMUT in accordance with the prior art;

Figure 2 is a sectional view of a single cell of a cMUT including an isolation post or area in accordance with the present invention;

Figure 3A – 3G shows the steps of fabricating a cMUT in accordance with the present invention;

Figure 4 is a sectional view of a cell of a cMUT with multiple isolation posts;

Figure 5 shows deflection of a membrane as a function of radius with a cMUT such as that shown in Figure 4;

Figure 6 shows capacitance voltage curves for cMUTs in accordance with the prior art and in accordance with the present invention; and

Figure 7 is a cross sectional view of a cell in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 2 illustrates one cell of a cMUT in accordance with the present invention. The same reference numbers have been applied to the like parts. The isolation layer, Figure 1, is replaced by an isolation post 18 which limits the excursion of the top membrane 12 to prevent shorting while limiting the accumulation of charge. The proper location and height or thickness of the isolation post will prevent shorting between the two electrodes within the device voltage operating range. The isolation posts or areas need to have a thickness such that the electric field across the posts or areas does not result in breakdown of the post materials. Since the post area is very small the charging problem is minimized to negligible value. The location and height of the small post can be designed to the shape of the deflection of the membrane as will presently be described. It is apparent, as will be described, that more than one post or area can be used. It will also be apparent that the isolation area can have any size, shape and height that prevents shorting during operation while reducing the number of trapped charges as compared to a non-patterned isolation layer.

An example of a process for forming cMUT with cells including isolation posts or areas is shown and described with regard to Figures 3A-3G. For example, the process may start with an n type silicon wafer 21 Figure 3A. The wafer can be heavily doped as, for example, with antimony to achieve a low resistance, for example, in the range of 0.008 to 0.020 ohm-centimeters square. Depending on the required electrodes separation of the cMUT one or two different processes form shallow or deep cavities before wafer bonding. When the separation distance between electrodes is less than two micrometers one can use a thermal oxide layer which is etched to form the cavity. A layer 22 of thermal oxide is grown and patterned using convention photolithography and etched to define the wells 23. If the depth of the wells 23 is to be larger than 2 micrometers the wafer is processed by selectively etching the silicon substrate 21 at the bottom of the wells to increase the depth. After the wells have been formed another

thermal oxide layer is grown and patterned using conventional photolithography to leave oxide posts or areas 24 at the bottom of the wells, Figure 3B. It should be understood that the areas can be patterned to have any size and shape. The height of the posts or areas is determined by the thickness of the oxide layer. The wafer with cavities is then bonded to a SOI wafer 26 under vacuum as shown in Figure 3C. Wafer bonding can be done with a bonder at approximately 1 x 10^{-5} microbar vacuum at 150 degrees. The bonded wafers are annealed at 1100 degrees centigrade for two hours. The wafer is ground and etched back through the oxide layer 27 leaving a silicon membrane 28. The active silicon layer 28 on the SOI wafer now constitutes the membrane 28 for the cMUT transducer. The thickness of the active silicon layer 28 becomes the membrane thickness and can be easily controlled. To gain electrical access to the carrier silicon wafer 21 openings 29 in the membrane, silicon and insulting silicon oxide layer is formed by masking and etching. Subsequently a thin film of aluminum 31 is sputtered and patterned to establish a connection to the top electrodes and to the substrate. A thin layer of low temperature oxide 32 then is deposited as a passive layer. Finally, the low temperature oxide layer is patterned and etched to create pads 33 for wire bonding.

Although a silicon substrate and a silicon membrane has been described the same bonding process can be used to fabricate cMUTs with other types of membranes such as silicon nitride, sapphire, diamond, etc. with other substrates such as silicon nitride substrates or other materials and with other insulating isolation materials.

Referring now to Figure 4 which illustrates a single cell of a cMUT with a silicon membrane 36 the design and location of the posts is described. The device includes two sets of posts. The location and height of the posts is determined by simulating the membrane deflection under electrostatic force. This is illustrated for the circular cell of Figure 4. It is apparent that the concept of isolation posts or areas can be applied to any membrane shape in any kind of post design. Furthermore, isolation posts or areas of different sizes, shapes, locations, and heights will allow engineering the variation of capacitance of the cMUT as a function of applied voltages. The location, size and height of the posts or areas can be chosen to optimize the frequency response, or the output pressure and receive sensitivity both before and after contact with the posts or areas.

Figure 5 shows how the location of the first and second set of posts shown in Figure 4 is determined. Figure 5 shows the membrane deflection for the cMUT of Figure 4 and the points of

maximum deflection where the post needs to be located. Figure 6 shows the capacitance as a function of voltage for cMUT's with and without isolation posts. It shows that a cMUT with isolation post (s) can operate over a fuller capacitive range without a pull-in effect by implementing properly designed post(s). Generally the capacitive change for received ultrasonic pressure is very small. Therefore, it is desired for the cMUT to operate very close to its collapse voltage to achieve optimum sensitivity. However, a large AC voltage is needed for a cMUT to transmit the maximum ultrasonic energy to the medium. This makes it almost impossible for the cMUT with a fully covered isolation layer to operate around its collapse voltage reliably due to the pull-in and effect. The monotonic behavior of the CV curve of the new cMUT with isolation posts overcomes the problem. Therefore the cMUT performance can be optimized for both transmission and reception by setting the bias voltage very close to the collapse voltage of the cMUT. The foregoing description illustrates the ability to obtain variations of capacitance and hence displacement as a function of applied voltage.

It is apparent that the isolation posts shown in Figure 4 could be applied to this top electrode membrane prior to bonding and operation would be the same. Figure 7 illustrates an embodiment of the invention in which the isolation posts 41 are fabricated on the membrane.

Thus there is provided cMUTs in which the shorting of the electrodes is prevented by isolation posts or areas which minimize the accumulation of charge which degrades the reliability and repeatability of device performance. The operation of the cMUT is vastly improved.